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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,183	02/02/2000	Junichi Hikita	P3213-9038	5846

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Arent Fox Kinter Plotkin & Kahn PLLC  
David T. Nikaido  
1050 Connecticut Avenue N. W.  
Suite 600  
Washington, DC 20036

EXAMINER

CRUZ, LOURDES C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 12/14/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/496,183

Applicant(s)

HIKITA ET AL.

Examiner

Lourdes C. Cruz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 8-12 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 10-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claims 8-9 are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☒ All b) ☐ Some \* c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☒ received.
2. ☐ received in Application No. (Series Code / Serial Number) \_\_\_\_\_.
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

## Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

This Office Action is in response to CPA filed 10-26-01.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Wenzel et al. (U.S. Patent No. 6150724).

Regarding claims 1, 3, and 4 Wenzel discloses (See Figs. 5,7, and 18) a semiconductor device comprising a first semiconductor chip 102 and a second semiconductor chip 104 superposed on and bonded to a surface of the first semiconductor chip, wherein in a region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip, chip connection portions (corresponding to 108) are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips; and wherein on the second semiconductor chip, chip connection portions are arranged in standardized positions so as to fit the chip connection portions arranged on the first semiconductor chip; wherein at least part of the chip connection portions arranged on the first

semiconductor chip are common to the plurality of predetermined types of chips so as to be used for input /output signals.

See that the prior art recites all the structural limitation above. The claim as amended, however, recites an intended use in conjunction with other structural limitations. Such limitations include, for example, the recitation of "input/output signals having identical specifications". This quoted intended use limitation does not distinguish the claimed invention from that disclosed by the prior art since the device of the prior art could be used with predetermined types of chips so as to be used for input/output signals having identical specifications.

Regarding claims 2 and 5 Wenzel discloses semiconductor chips with identical functions but of different grades in as much as any specific function is claimed.

Wenzel also teaches a chip connection region wherein chip connection portions (corresponding to 108) are formed in standardized portions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connecting portions are arranged:

- Along an edge (left corner) of the chip connection region (Claim **10**)
- Along an edge and in an inner portion of the chip connection region (Claim **11**)
- Along an edge of the chip connection region, which is rectangular in shape, and also along opposite sides of the chip connection region (Claim **12**)

***Response to Arguments***

Applicant's arguments filed 10-26-01 have been fully considered but they are not persuasive.

Applicant has requested clarification regarding withdrawal of consideration of claim 9.

Claim 9 is directed to distinct invention. See quote from previous Office Action below:

"Newly submitted claims 8 and 9 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The claim recites limitations of a method for forming a semiconductor device, which constitutes a different invention than that which was originally presented by the applicant. The originally presented invention and the invention of claims 8 and 9 are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f))."

In the case of claim 8, the device as claimed could be made by forming connections in standardized and non-standardized among said chips, then discarding the non-standardized connections by removing such.

Applicant argues that:

- Wenzel fails to disclose or suggest chip connection portions arranged in standardized positions so as to fit any of a plurality of types of semiconductor chips.

- Applicant Argues that the prior art does not disclose the claimed device “wherein at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of chips so as to be used for input /output signals having identical specifications”

These arguments are not persuasive since:

- Wenzel (Figure 18) in Col. 13 clearly discloses chip connection portions arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips.
- See rejection above where the examiner has pointed out that the Prior art discloses chip connection portions –corresponding to 108-- on the first chip wherein these connection portions are used for input/output signals
- The phrase “predetermined” does not distinguish the invention from the prior art since the prior art uses pre-determined types of chips as well.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lourdes C. Cruz whose telephone number is 703-306-5691. The examiner can normally be reached on M-F 8:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Lourdes Cruz  
December 12, 2001

Lourdes C. Cruz  
Examiner  
Art Unit 2815



**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**